

## Programmable Logic University Of California Berkeley

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[logic arrays](#) University of California, Irvine University of California at Irvine Mechanical Systems Laboratory Data Acquisition Note: These notes are derived from Ch 8 Data Acquisition, Introduction to Mechatronics and a programmable logic controller (PLC), which is a specialized industrial device for interfacing to

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University of California, Los Angeles ABSTRACT The programmable logic block (PLB) in a modern FPGA features a built-in carry chain (or adder) and a decomposable LUT, where such an LUT may be decomposed into two or more smaller LUTs Leveraging

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Researchers at UCLA have developed a fault-tolerant logic resynthesis algorithm for LUT-based FPGAs which decreases the circuit fault rate without changing the topology of the logic network, thus eliminating the additional rounds of physical design that are required in conventional resynthesis algorithms.

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This course covers the logic theory and application of programmable logic controllers (PLCs). The material focuses on the design and development of programming algorithms used to interact with motors, sensors, switches, networks, valves, relays, and hydraulic and pneumatic systems. The focus is on Allen Bradley and Rockwell Automation software although Siemens PLCs will be explained as well.

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Logic Friday is a free Windows program that provides a graphical interface to Espresso, as well as to mist1, another module in the Berkeley Octools package. With Logic Friday users can enter a logic function as a truth table, equation, or gate diagram, minimize the function, and then view the results in both of the other two representations.

[Espresso heuristic logic minimizer - Wikipedia](#)  
University of California, Berkeley Technical Report No. UCB/ERL M93/80 November 1993 <http://www2.eecs.berkeley.edu/Pubs/TechRpts/1993/ERL-93-80.pdf>. Field programmable logic devices (FPLDs) are fast emerging as viable alternatives to mask programmed parts because of their rapid time-to-market and low costs.

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